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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/469,754	12/22/1999	YASUTAKA TSUKAMOTO	2271/53999-A	5345

7590 06/22/2004

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	16

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/469,754	TSUKAMOTO ET AL.
	Examiner	Art Unit
	Dwin M Craig	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-39 have been presented for reconsideration in view of Applicant's Request for Reconsideration under 37 C.F.R. 1.114 and Applicant's amended claim langauge.

Response to Arguments

2. Applicant's arguments filed on 4-5-2004 have been fully considered. Examiners response is as follow:

2.1 Regarding the Applicant's response to the 35 U.S.C. 103 rejections of Claims 1-39 in view of *Messerman et al.* and *Dangelo et al.* and *Koza et al.* and *Microsoft Press Computer Dictionary*:

The Applicants have argued:

> Regarding the obviousness rejection based on Messerman as a primary reference, Applicants respectfully submit that the claims of this application cannot be obvious in view of a combination of references in which Messerman is the primary reference, since Messerman is not within the scope of the relevant art.

The Examiner agrees with Applicant, in regards to the *Messerman* reference. Applicant's arguments are persuasive and the Examiner withdraws the 35 U.S.C. 103 rejections of Claims 1-39 in view of *Messerman et al.* and *Dangelo et al.* and *Koza et al.* and *Microsoft Press Computer Dictionary.*

2.2 Regarding the Applicant's response to the 35 U.S.C. 103 rejections of Claims 1-39 in view of *Raman et al.* and *Crafts et al.* and *Dangelo et al.*

Applicant argued:

> Crafts was cited in the Office Action as purportedly disclosing calculating the alternating current component of each cell.
> However, Applicant's find no teaching or suggestion in Crafts of estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operating frequency for each logic state, and determining an alternating current component and a direct current

component for each logic state to calculate the current consumed by the mega cells.

The Examiner asserts, for the limitation of calculating the power consumption of the Mega-cells, the *Raman et al.* reference was relied upon ***(Col. 6 Lines 56-67, Col. 7 Lines 1-4).*** The Examiner reviewed the *Craft et al.* reference and determined that an artisan of ordinary skill, would know to calculate the average operating frequency of an operating cell, as taught by the *Craft et al.* reference **(Col. 3 Lines 18-28).** Specifically, the calculation of the dynamic switching rate of the logic cells **(Figures 3 & 5),** reads directly on Applicant's claimed limitation of determining the average operating frequency for each logic state.

Applicant argued:

However, Applicants simply does not find teaching or suggestion in the cited art of estimating power consumption of an integrated circuit which includes estimating a current consumed by the mega cells by obtaining logic states for each logic state, and determining an average operation frequency for each logic state for each mega cell, determining an alternating current component and a direct current component fro each logic state to calculate the current consumed by the mega cells, as recited in independent claim 1.

The Examiner has argued that the combination of the reference teaches all of the claimed limitations.

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

The Examiner has found Applicants arguments to be unpersuasive and uphold the rejections of Claims 1-39 under 35 U.S.C. 103.

An updated search has revealed new art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Independent **Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Brasen et al. U.S. Patent 5,481,469** in view of **McNelly et al. U.S. Patent 5,625,803.**

3.1 As regards independent **Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39** the *Brasen et al.* reference discloses, a method of estimating power consumption of an IC **(Col. 1 Lines 28-38),** simulating logic of basic and mega-cells **(Figures 7&8),** estimating a first value of electric power consumed by the mega-cell, with pre-established data **(Block 2 Figure 8 and Figure 6, Col. 3 Lines 14-23).**

However, the *Brasen et al.* reference does not expressly disclose calculation of alternating current component.

The *Brasen et al.* reference discloses that there is a need in the art for accurate calculation of the power dissipation of logic elements **(Col. 2 Lines 1-4).** An artisan of ordinary skill, would have been motivated, to search the electronic design arts to find a method of accurate calculation of the power dissipation of logic elements as suggested by the *Brasen et al.* reference. In the integrated circuit design art, the *McNelly et al.* reference discloses a method of accurate calculation of the power dissipation of logic elements, specifically the alternating current component **(Figure 7, Col. 2 Lines 32-38).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the integrated circuit power estimation methods of the *Brasen et al.* reference with the integrated circuit power estimation methods of the *McNelly et al.* reference because, the use of the methods disclosed in the *McNelly et al.* reference will provide for more accurate power consumption data for IC design and thus provide the desiger with a model of how the finished IC will perform **(McNelly et al. Col. 2 Lines 33-46).**

4. **Claims 1- 39** are rejected under 35 U.S.C. 103(a) as being unpatentable in view of **Raman et al. U.S. Patent 5,535,370** in view of **Crafts et al. U.S. Patent 5,521,834** and in further view of **Dangelo et al. U.S. Patent 5,493,508.**

4.1 As regards **Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39** the *Raman et al.* reference discloses a method of calculation of power using a circuit simulation **(Figures 1-3),** using a lookup table with pre-established power consumption data **(Figure 1 Item 50, Col. 4 Lines 59-65),** for each logic state **(Figures 4(a), 4(b)),** determining the average operation frequency **(Figure 1 Item 20, Col. 1 Lines 50-64),** determining a direct current for each node **(Figure 3**

Item 220, Figures 4(c) and 4(d), 6b, 7, Col. 1 Lines 65-67, Col. 2 Lines 1-31), basic cells **(Col. 4 Lines 66-67, Col. 5 Lines 1-52),** and portions of a mega cell **(Col. 6 Lines 56-67, Col. 7 Lines 1-4).**

The *Ramen et al.* reference does not expressly disclose calculating the alternating current component for each cell.

The *Crafts et al.* reference discloses calculating the alternating current component for each cell **(Figure 2 Items 30, 32, 34, Col. 4 Lines 1-67, Col. 5 Lines 1-10).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Ramen et al.* reference with the *Crafts et al.* reference because, the *Crafts et al.* reference discloses a better approach that is more accurate to calculate the power dissipated in a CMOS IC ***(Crafts et al. Col. 6 Lines 31-62).***

The *Ramen et al.* reference does not expressly disclose mega-cells and hardware description languages.

The *Dangelo et al.* reference discloses mega-cells **(Col. 11 Lines 1-4),** and hardware description languages **(Col. 11 Lines 49-55).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention to have modified the *Ramen et al.* reference with the *Dangelo et al.* reference because, *(motivation to combine)* the *Dangelo et al.* reference discloses an improved method of simulating mega-cells with a hardware description language *(Dangelo et al. Col. 4 Lines 13-67).*

4.2 As regards independent **Claims 25, 29, 30, 33, 34, 37, 38 and 39** the *Ramen et al.* reference does not expressly disclose a programmable computer.

The *Craft et al.* reference discloses a programmable computer **(Figure 1).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Ramen et al.* reference with the *Crafts et al.* reference because, the *Crafts et al.* reference discloses a better approach that is more accurate to calculate the power dissipated in a CMOS IC ***(Crafts et al. Col. 6 Lines 31-62).***

4.3 As regards independent **Claims 1, 9 and 17** the *Ramen et al.* reference does not expressly disclose a computer readable medium with computer executable code.

The *Dangelo et al.* reference discloses a computer readable medium with computer executable code **(Col. 8 Lines 47-67).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention to have modified the *Ramen et al.* reference with the *Dangelo et al.* reference because, the *Dangelo et al.* reference discloses an improved method of simulating mega-cells with a hardware description language ***(Dangelo et al. Col. 4 Lines 13-67).***

Conclusion

5. **Claims 1-39** are rejected.

5.1 This action is **NON-FINAL.**

5.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC